

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: MURATA, et al.  
Serial No.: Not yet assigned  
Filed: January 14, 2004  
For: A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A  
METHOD OF MANUFACTURING THE SAME

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR 1.97 & 1.98**

Mail Stop DD  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

January 14, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

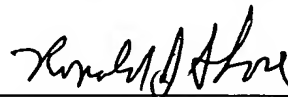
Although some of the documents listed on the attached form equivalent to Form PTO-1449 are not in the English language, the requirement of 37 CFR 1.98(a)(3) for a concise explanation of the relevance is satisfied by the attached English language abstracts.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (Case: 501.43228X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS LLP



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Attachments

<b>Form PTO-1449</b>	<b>U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE</b>	<b>ATTY. DKT. NO.</b> 501.43228X00	<b>SERIAL NO.</b>
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use several sheets if necessary)		<b>APPLICANT</b> MURATA, et al.	
		<b>FILING DATE</b> January 14, 2004	<b>GROUP</b>

**U.S. PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA	5,198,683	03/30/1993	SIVAN	357	67	05/03/1991
AB	5,670,803	09/23/1997	BEILSTEIN, Jr. et al.	257	278	02/08/1995
AC	5,994,735	11/30/1999	MAEDA, et al.	257	329	11/30/1999
AD	5,627,390	05/06/1997	MAEDA, et al.	257	302	05/06/1997
AE						
AF						
AG						
AH						
AI						
AJ						
AK						
AL						

**FOREIGN PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Country	Class	Subclass	Abstract	
						Yes	No
AM	11-176936	07/02/1999	JP	H01L	21/768	X	
AN	9-232447	09/05/1997	JP	H01L	21/8244	X	
AO	2001-28443	01/30/2001	JP	H01L	29/786	X	
AP	6-104405	4/15/1994	JP	H01L	27/11	X	
AQ	03/019663	03/06/2003	WO	H01L	27/11		
AR	00/70683	11/23/2000	WO	H01L	27/108		
AS							
AT							

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
AV	
AW	
AX	
AY	
AZ	
<b>Examiner</b>	
<b>Date Considered</b>	